Hierarchical Design

ECE 09414 - 2 VLSI

Dr. Hanafi

Everett Jones

10/10/17

I. Introduction

The purpose of this lab was to understand the function of utilizing multiple inverters to create a delay in a circuit. This also expanded on how these transistors can be modified through variables to fit needs in the circuit. This allows for the width and length to be changed without having to go through each schematic to make these updates when testing the circuits developed.

II. Procedure

Using the copy cell feature the inverter schematic previously created was duplicated four times in order to make a set of inverters that allowed for scaled sizes of widths and lengths. The length and width of the nmos and the pmos transistors in each of the inverters controlled by variables that were later defined in the simulation setup. After running through with static parameters for these variables the graph in Figure 2 was created which shows the signal as it is passed through each of the inverters. For the final step of the process the nmos and pmos ratio was varied from one to three in steps of 0.2. The graph created for these various points can be seen in Figure 3.

III. Results

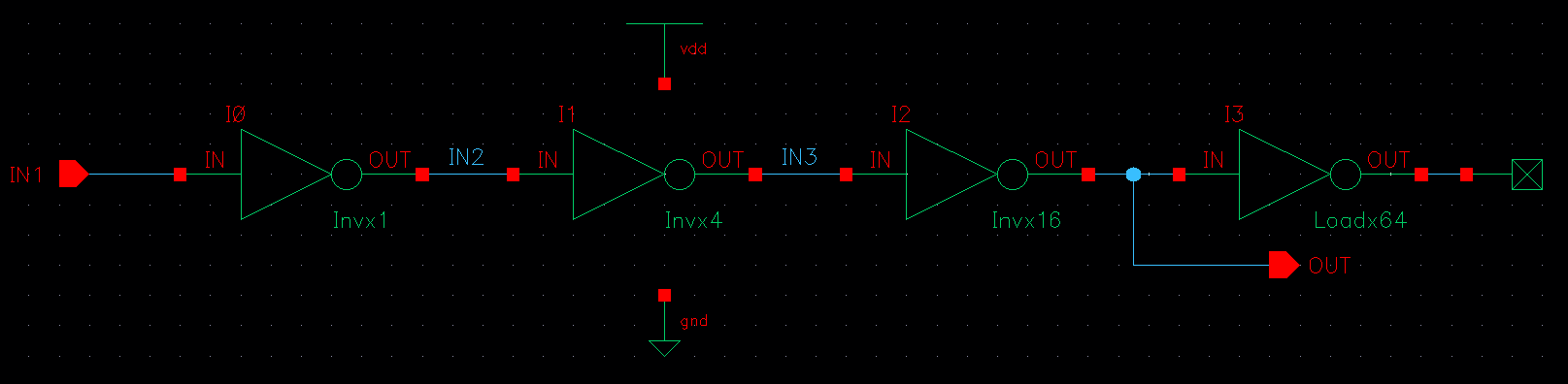


Figure 1: Inverters in a cascading order, scaling the inverters from 1 to 64 times scale.

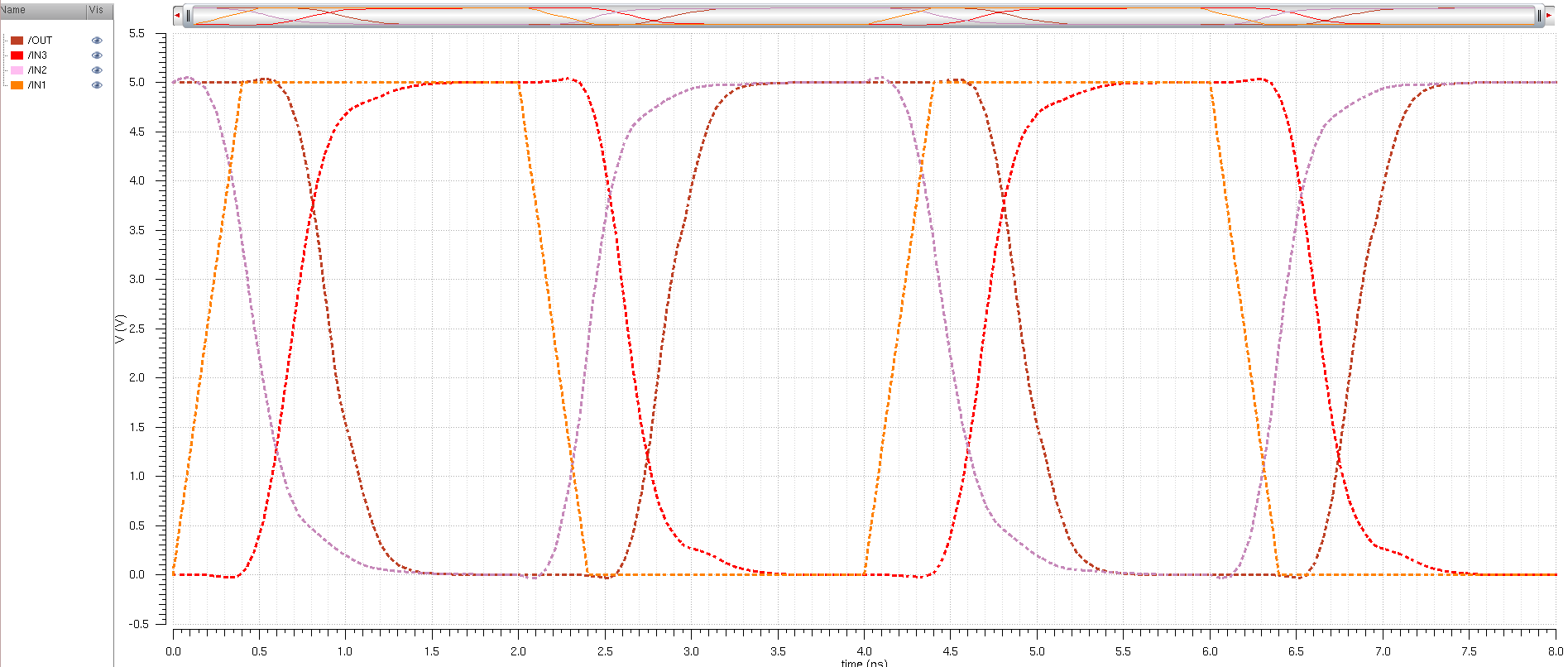


Figure 2: The signal as it passes through each of the inverters until it reaches the output. The signal can be seen to be delayed from input to output by roughly 0.7ns.

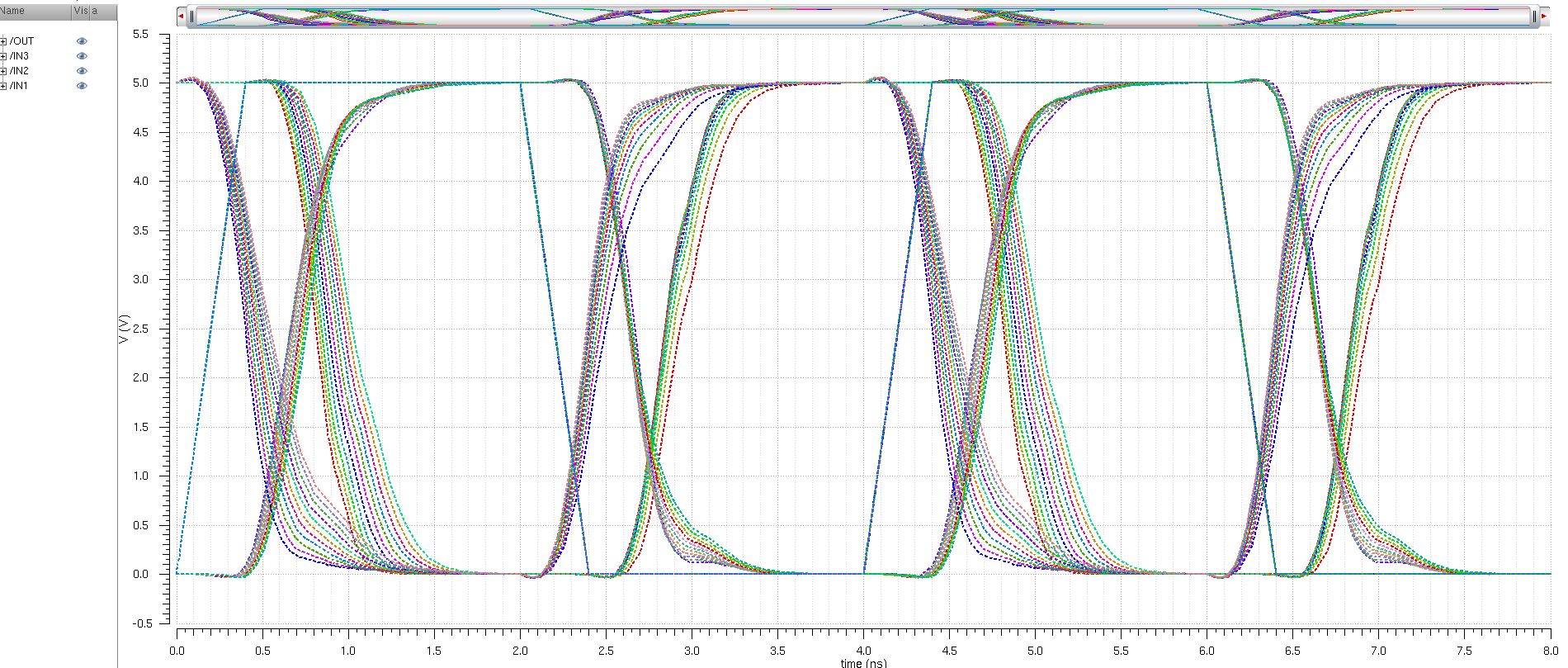


Figure 3: The signal as it passes through the delay circuit. The pmos/nmos ratio varying from one to three in steps of 0.2. The transition from high to low can be seen to be more efficient as the ratio is lower whereas the transition from low to high can be seen to be more effective as the ratio reaches 1.5.

IV. Conclusions

From the graphs created from the simulations done on the inverter delay circuit it can be seen that the rising and falling time of the signal varies greatly with the pmos/nmos ratio. The smaller the ratio is the lower the fall time is, but as the ratio grows slightly bigger the rise time begins to shorten as well. This would mean that to have an efficient system a compromise would have to be made in regards to the ratio used, but most importantly in the width of the transistor. With the length being a fixed value the width would have to change accordingly to accommodate for an efficient rise and fall time for the signal.